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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/651,924	08/31/2000	Michael S Bertone	1662-31400 (P00-3212)	4257

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EXAMINER	
NGUYEN, DUSTIN	
ART UNIT	**PAPER NUMBER**
2154	

DATE MAILED: 08/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/651,924	BERTONE ET AL.	
	Examiner	Art Unit	
	Dustin Nguyen	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 24 are presented for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 14-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shah et al. [US Patent No 6,347,337], in view of Barkey et al. [US Patent No 6,044,406].

4. As per claim 14, Shah discloses the invention substantially as claimed including a method of allocating space in a shared buffer, comprising:

assigning credits to each of a plurality of sources that sends data packets to the shared buffer [i.e. each end point consists of descriptors, buffers and information for credit-based flow control] [20, Figure 1A; col 7, lines 50-63; and col 12, lines 6-12];

wherein if the number of empty buffer spaces is larger than a buffer threshold, automatically paying the credit back to the source from which the credit and data were sent [Abstract; col 15, lines 36-41]; and

wherein if the number of empty buffer spaces is smaller than the buffer threshold, holding the credit until a buffer space becomes empty and then paying a credit back to a source from which a credit was sent [i.e. pending] [Abstract; col 15, lines 42-48; and col 16, lines 42-52].

Shah does not specifically disclose

requiring each source to spend a credit each time that source sends data packets to the shared buffer.

Barkey discloses

requiring each source to spend a credit each time that source sends data packets to the shared buffer [i.e. decrement] [col 4, lines 26-38].

It would have been obvious to a person skill in the art at the time the invention was made to combine the teaching of Shah and Barkey because Barkey's teaching of decrementing the number of credit would have enable flow control to prevent traffic congestion to increase system performance.

5. As per claim 15, Shah discloses when the number of empty buffer spaces is smaller than the buffer threshold and a buffer space becomes empty, automatically returning a credit in a random, equally probable manner to one of the sources which have spent credits held by the buffer [i.e. creditresponse is sent to other end point] [col 15, lines 36-41].

6. As per claim 16, Shah discloses when the number of empty buffer spaces is smaller than the buffer threshold and a buffer space becomes empty, automatically returning a credit in a

random, statistically skewed manner to one of the sources which have spent credits held by the buffer [col 12, lines 60-col 13, lines 18].

7. As per claim 17, Shah does not specifically disclose assigning a minimum number of credits to each source that is sufficient to allow each source to send a continuous sequence of data packets without waiting for return credits. Barkey discloses assigning a minimum number of credits to each source that is sufficient to allow each source to send a continuous sequence of data packets without waiting for return credits [col 4, lines 57-col 5, lines 5]. It would have been obvious to a person skill in the art at the time the invention was made to combine the teaching of Shah and Barkey because Barkey's teaching would allow to fully utilize the bandwidth for information transferring.

8. As per claim 18, Barkey discloses preventing a source from delivering a data packet to the shared buffer if that source has no available credits [i.e. wait for available credit] [col 8, lines 52-61].

9. As per claim 19, Barkey discloses setting the buffer threshold equal to the number of total credits assigned to all the sources [col 4, lines 58-66].

10. As per claim 20, Barkey discloses using a counter in each source and a counter for each source coupled to the buffer to track spent and paid back credits [30, 32, Figure 1; and col 4, lines 26-38].

11. As per claim 21, it is rejected for similar reasons as stated above in claim 14.

12. As per claim 22, Shah discloses wherein each credit corresponds to a single memory request [col 2, lines 1-3].

13. As per claim 23, Shah discloses a buffer adapted to receive a plurality of memory requests from said sources, and said credits are automatically issued to said sources to permit said sources to provide said requests to said buffer [20, Figure 1A; and col 2, lines 12-26].

14. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shah et al. [US Patent No 6,347,337], in view of Barkey et al. [US Patent No 6,044,406], and further in view of Tiainen et al. [US Patent No 6,674,722].

15. As per claim 24, Shah and Barkey do not specifically disclose the receiver issues credits among said sources to avoid a source from having exclusive access to said receiver to the exclusion of the other sources. Tiainen discloses the receiver issues credits among said sources to avoid a source from having exclusive access to said receiver to the exclusion of the other sources [i.e. distributed credit] [col 3, lines 25-28]. It would have been obvious to a person skill in the art at the time the invention was made to combine the teaching of Shah, Barkey and

Tiainen because Tiainen's teaching would allow to control the flow of data messages between distributed multiprocessor system.

16. Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shah et al. [US Patent No 6,347,337], in view of Barkey et al. [US Patent No 6,044,406], and further in view of Shimizu [US Patent No 6,715,008], and Deneroff et al. [US Patent No 6,751,698].

17. As per claim 1, it is rejected for similar reasons as stated above in claim 14. Furthermore, Shah and Barkey do not specifically disclose a plurality of processors, each processor coupled to at least one memory cache, one cache control unit, and one interprocessor router; and a memory coupled to each processor, each memory managed by a memory controller configured to accept memory requests from the plurality of processors; wherein the memory requests from a local processor are delivered to the memory controller by the cache control unit and wherein memory requests from other processors are delivered to the memory controller by the interprocessor router.

Shimizu discloses

a plurality of processors [Figures 1 and 2], each processor coupled to at least one memory cache [204, Figure 2]; and one interprocessor router [220, Figure 2; and col 3, lines 25-48]; and

a memory coupled to each processor [206, Figure 4], each memory managed by a memory controller configured to accept memory requests from the plurality of processors [356, Figure 4]; and

wherein memory requests from other processors are delivered to the memory controller by the interprocessor router [Figure 4; and col 3, lines 66-67].

Shah, Barkey and Shimizu do not specifically disclose

one cache control unit, and

wherein the memory requests from a local processor are delivered to the memory controller by the cache control unit.

Deneroff discloses

one cache control unit, and wherein the memory requests from a local processor are delivered to the memory controller by the cache control unit [i.e. directory controller provides cache functions] [col 2, lines 32-40].

It would have been to a person skill in the art at the time the invention was made to combine the teaching of Shah, Barkey, Shimizu and Deneroff because Deneroff's teaching of cache would allow to reduce communication overhead and increase system performance.

18. As per claim 2, it is rejected for similar reasons as stated above in claim 14. Furthermore, Shimizu discloses wherein:

the interprocessor router are each assigned a number of credits [col 5, lines 56-57];

at least one of said credits must be delivered by the interprocessor router to the memory controller when a memory request is delivered by the interprocessor router to the memory controller [col 5, lines 19-27].

Deneroff discloses

the cache control unit are each assigned a number of credits [col 42, lines 29-32];

at least one of said credits must be delivered by the cache control unit to the memory controller when a memory request is delivered by the cache control unit to the memory controller [col 42, lines 38-67].

It would have been obvious to a person skill in the art at the time the invention was made to combine the teaching of Shimizu, Deneroff because Deneroff's teaching would allow to manage buffer and control the flow to prevent traffic congestion.

19. As per claim 3, it is rejected for similar reasons as stated above in claims 14 and 18.

20. As per claim 4, it is rejected for similar reasons as stated above in claim 17.

21. As per claim 5, Shah discloses the number of credits spent by the cache control unit and the interprocessor router are stored and updated in counters located in the shared buffer [i.e. registers] [col 10, lines 62-col 11, lines 9]. Shah and Barkey do not specifically disclose the number of credits available in the cache control unit and the interprocessor router are stored and updated in counters located in the cache control unit and the interprocessor router. Shimizu discloses the number of credits available in the cache control unit and the interprocessor router are stored and updated in counters located in the cache control unit and the interprocessor router [i.e. credit registers] [302, Figure 3; Abstract; and col 4, lines 1-5]. It would have been obvious to a person skill in the art at the time the invention was made to combine the teaching of Shah, Barkey and Shimizu because Shimizu's teaching would allow to control traffic flow in a more efficient manner.

22. As per claim 6, Barkey discloses the threshold is the point when the number of free spaces available in the buffer is equal to the total number of credits assigned to the cache control unit and the interprocessor router [col 10, lines 26-49].

23. As per claim 7, it is rejected for similar reasons as stated above in claims 1 and 2. Furthermore, Shah, Barkey and Shimizu do not specifically an associated memory, a request buffer in a front-end directory in-flight table, an L2 data cache; an L2 instruction and data cache control unit configured to send request and response commands from the processor to the memory controller; and an interprocessor and I/O router unit configured to send request and response commands from remote processors to the memory controller. Deneroff discloses an associated memory, a request buffer in a front-end directory in-flight table, an L2 data cache; an L2 instruction and data cache control unit configured to send request and response commands from the processor to the memory controller; and an interprocessor and I/O router unit configured to send request and response commands from remote processors to the memory controller [col 2, lines 32-57; and col 47, lines 36-38]. It would have been obvious to a person skill the art at the time the invention was made to combine the teaching of Shah, Barkey, Shimizu and Deneroff because Deneroff's teaching of L2 cache would provide additional level of caching to increase system performance.

24. As per claim 8, it is rejected for similar reasons as stated above in claims 2 and 3.

25. As per claim 9, Shimizu discloses the credits are returned to the sources which have given up credits to the directory in-flight table in a random, equally probably manner [col 3, lines 50-65].

26. As per claim 10, it is rejected for similar reasons as stated above in claims 6 and 7.

27. As per claims 11 and 12, they are rejected for similar reasons as stated above in claims 5 and 7.

28. As per claim 13, it is rejected for similar reasons as stated above in claim 4. Furthermore, Shah discloses wherein the number of credits available to the L2 instruction and data cache control unit and interprocessor and I/O router is determined by the round trip time required to send a credit to and receive a credit from the directory in-flight table [col 9, lines 24-42].

29. Applicant's arguments with respect to claims 1-24 have been considered but are moot in view of the new ground(s) of rejection.

30. A shortened statutory period for response to this action is set to expire **3 (three) months and 0 (zero) days** from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 U.S.C 133, M.P.E.P 710.02, 710.02(b)).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dustin Nguyen whose telephone number is (571) 272-3971. The examiner can normally be reached on flex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Follansbee John can be reached on (571) 272-3964. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dustin Nguyen
Examiner
Art Unit 2154

LARRY D. DONAGHUE
PRIMARY EXAMINER